#8/4
7/30/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Celii et al.
Serial No.: 09/599,718
Filing Date: 06/22/00
Title: PROCESS FLOW FOR DUAL DAMESCENE INTERCONNECT STRUCTURES

Art Unit: 1765
Examiner: Brown, C.
Docket No.: TI-29276

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Amendment under 37 CFR 1.115

Assistant Commissioner of Patents
Washington, DC 20231

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated 02/28/02. They are respectfully submitted as a full and complete response to that Action.

Please amend the above-referenced application as follows:

In the Claims:

Amend Claim 1 to read as follows:

1. (amended) A method of fabricating an integrated circuit, comprising the steps of:

forming an interlevel dielectric layer over a semiconductor body;
forming an intrametal dielectric layer over said interlevel dielectric layer;
forming a hardmask over said intrametal dielectric layer;
forming a via pattern over said hardmask;
selectively etching a via through said hardmask;
extending said via by selectiv ly etching said intrametal dielectric layer;

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From:
Texas Instruments Incorporated
Facsimile: 972-917-4418
Phone: 214-532-9348

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CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at **703-872-9310** on the date shown below:

Jacqueline J. Garner, Reg. No. 36,144 — July 29, 2002 Date

FACSIMILE COVER SHEET

X FACSIMILE COVER SHEET	X AMENDMENT (6 Pages)
___ NEW APPLICATION	X EOT 2mth (3 Pages)
___ DECLARATION (# Pages)	___ NOTICE OF APPEAL (# Pages)
___ ASSIGNMENT (# Pages)	___ APPEAL (# Pages)
___ FORMAL DRAWINGS	___ ISSUE FEE (# Pages)
___ INFORMAL DRAWINGS	___ REPLY BRIEF (IN TRIPLICATE) (# Pages)
___ CONTINUATION APP'N (# Pages)	___
___ DIVISIONAL APP'N	

NAME OF INVENTOR(S): Celii	RECEIPT DATE & SERIAL NO.: **Serial No.: 09/599,718** **Filing Date:** 06/22/2000
TITLE OF INVENTION: Process Flow for Dual Damescene Interconnect	
TI FILE NO.: TI-29276 / DEPOSIT ACCT. NO.: **20-0668**	
FAXED: 7/29/02 DUE: 5/28/02 ATTY/SEC'Y: JJG	

Texas Instruments Incorporated
PO Box 655474, M/S 3999
Dallas, TX 75074